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change, *i.e.*, increase or decrease.

An electrically programmable resistance, non-volatile memory device, operable at room temperature, was made of PCMO epitaxially grown on YBCO on $LaAlO_3$, as published by Liu *et al*. This type of memory may be reversibly programmed by a reversed short electrical pulse. The memory cell is able to produce either single bit or multi-bit information. However, the PCMO must be in crystalline form, which requires that the PCMO must be grown on a specific bottom electrode, such as YBCO, which is not compatible to the state-of-the-art silicon integrated circuit technology. The growth, or crystallization, temperature is relatively high, *e.g.*, >700°C, which makes integration of the device into state-of-the-art integrated circuit very complex. In addition it is not possible to cover the full circuit area with a single grain of PCMO. As the properties of a memory cell which is fabricated on a single grain PCMO crystal and the properties of a memory cell which is fabricated on a multi-grain PCMO crystal, which covers the grain boundary area, are not the same, circuit yield and memory performance problems will occur.

Summary of the Invention

A method of fabricating a variable resistance device, wherein the resistance is changed by passing a voltage of various pulse ~~length~~ lengths through the device, includes preparing a silicon substrate; forming a silicon oxide layer on the substrate; depositing a first metal layer on the silicon oxide, wherein the metal of the first metal layer is taken from the group of metals consisting of platinum and iridium; depositing a perovskite metal oxide thin film on the first metal layer; depositing a second metal layer on the perovskite metal oxide, wherein the metal of the second metal layer is taken from the group of metals consisting of platinum and iridium; annealing the structure at a temperature of between about 400°C to 550°C for between about ten minutes and

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Fig. 4 is a graph of R v. number of pulse measurements.

Detailed Description of the Preferred Embodiments

The method of the invention includes forming a PCMO metal oxide thin film on a substrate by spin-coating. PCMO thin films are polycrystalline and exhibit large reversible resistance changes when an electric pulse is applied.

The PCMO thin film of the method of the invention is deposited on a platinum or iridium layer which is in turn deposited on a silicon substrate, by a spin-coating process. A low temperature annealing process renders the PCMO thin film in a basic amorphous or polycrystalline structure. The resistance change is achieved by applying an electric pulse, and the character of the resistance change, *i.e.*, increase or decrease, depends on the duration time of electric pulse. The range of the resistance change is quite large, from as low as 400Ω to as high as 250 kΩ.

The method of the invention includes fabricating a memory resistor on an amorphous or on a very small grain PCMO thin film. Because the PCMO is in an amorphous form, it does not require a very high temperature treatment, and may be formed on a device bottom electrode, such as are used in state-of-the-art silicon integrated circuit processes. In addition, the amorphous PCMO material may be uniformly deposited over the full silicon wafer or in a nano-scale patterned area. These properties are essential for the method of the invention to be useful in very large scale memory chip and embedded memory integration applications.

Referring now to Fig. 1, the memory cell 10 of the invention is ~~fabrication~~ <u>fabricated</u> on a silicon substrate 12, which may be a bulk silicon or SIMOX substrate, and which has an oxide layer on the upper surface thereof. A layer of platinum 14 is deposited on the silicon substrate, and, in the preferred embodiment, is un-patterned. Layer 14 is deposited to a thickness of between

about 100 nm to 200 nm by electron beam deposition, or other suitable deposition techniques. Multiple layers of PCMO are spin coated onto platinum layer 14 to a desired thickness, which, in the preferred embodiment, is between about 100 nm to 300 nm. After each layer of PCMO film is spin coated, the structure is baked and annealed for between about five minutes and twenty minutes prior to the next coating process. During the baking process, in an ambient atmosphere, the temperature is progressively stepped up from about 100°C to about 250°C. For instance, the structure may be initially heated to about 120°C for one minute, then heated to about 180°C for about one minute, and then heated to about 240°C for about one minute. The structure is then annealed in an oxygen atmosphere at a temperature of between about 400°C to 700°C for the remainder of the time. The structure is then cooled, and the next layer of PCMO filmed is formed by spin coating. Typically, three layers of PCMO are deposited, although, the desired thickness may require between two and five layers. After the final layer is coated and baked, the stack of the film is annealed at low temperature in the range of between about 400°C to 700°C for between about five minutes to three hours in an oxygen atmosphere.

After the low temperature processing steps, the PCMO film is no longer in a single crystal form. The processed film includes an amorphous layer 16b and may include nano-meter size crystals in a bottom layer 16a. A top electrode 18 is fabricated of platinum, which is deposited through a ~~shallow~~ <u>shadow</u> mask, resulting in platinum buttons on the upper surface of the device. Layer 18 is deposited to a thickness of between about 100 nm to 200 nm by electron beam deposition, or other suitable deposition techniques. Top platinum dots 18, PCMO layer 16 and bottom platinum layer 14 form a PCMO resistor. The R-RAM device of the invention may be used in various forms ~~if~~ <u>of</u> integrated circuits or incorporated into other devices. The structure is completed by the usual

insulating and metallization steps.

A number of metal oxide compositions may be used to fabricate the memory device of the invention according to the method of the invention. The R-RAM metal oxide composition has the general formula of $M'_xM''_{(1-x)}M_yO_z$, wherein:

M': is taken from the group consisting of La, Ce, Bi, Pr, Nd, Pm, Sm, Y, Sc, Yb, Lu, Gd;
M": is taken from the group consisting of Mg, Ca, Sr, Ba, Pb, Zn, Cd;
M: is taken from the group consisting of Mn, Ce, V, Fe, Co, Nb, Ta, Cr, Mo, W, Zr, Hf, Ni;
x: has a range of between 0 to 1;
y: has a range of between 0 to 2; and
z: has a range of between 1 to 7.

The metal oxide thin film may be fabricated using any of several conventional techniques, including metal oxide sputtering, spin-coating and MOCVD, although spin-coating is the preferred technique. A voltage of 0.1V is applied between top platinum electrode 18 and bottom platinum electrode 14 for current and resistance measurement. The resistance is defined as the voltage divided by the current: R=V/I.

The data depicted in Figs. 2 and 3 was obtained ~~form~~ from a R-RAM device fabricated according to the method of the invention, and specifically, a PCMO thin film was deposited on a silicon substrate having a non-partitioned platinum layer thereon by a spin-coating process. The thickness of the thin film was about 250nm, as confirmed by SEM. The thin film composition was $Pr_{0.7}Ca_{0.3}MnO_3$. The resistance was measured on a HP-4145B semiconductor analyzer, and the electric pulse was generated from a pulse generator.

As shown in Figs. 2 and 3, an electric pulse of short duration, *e.g.*, 15 nsec to 1000 nsec, at between about two to five volts, with three volts being the preferred voltage, increases the

resistance while an electric pulse of longer duration, *e.g.*, 700 nsec to 1000 nsec, at between about one to three volts, with two volts being the preferred voltage, decreases the resistance. The pulse length and voltage are dependent on film thickness. The lowest measured resistance was about 400 Ω, and the highest measured resistance was about 250 kΩ. The resistance went up when the pulse duration was in a broad range of between about 3 nsec to 700 nsec, while the resistance went down when the pulse duration was in a broad range of between about 700 nsec to one second.

Fig. 4 depicts the resistance of the memory resistor of Fig. 1 after each pulse is applied. The y-axis is the memory cell resistance and the x-axis is the number of the measurement. The amplitude of the pulse is indicated in Fig. 4. First, a wide pulse of pulse width 1 msec is applied. The resistance of the resistor is about 200 ohm. Next a series of 10 narrow, *e.g.*, 5 nsec to 20nsec, pulses are applied. The resistance of the resistor is measured and recorded after each series of pulses. The resistance of the resistor increases as the number of narrow pulses is increased. Finally the resistance saturated at about 200 kOhm. When a longer pulse is applied, the resistance of the resistor drops to about 200 ohm. The resistance of the resistor increases again when additional short pulses are applied. Thus the resistor may be programmed using electric pulses of short duration. A wide width pulse of the same amplitude may be used to reset the memory. The number of narrow pulses may control the resistor of the memory cell. The memory cell may also be used as multi-bit memory cell.

It is particularly interesting that the resistance increases following narrow pulses as well as decreases following wide pulses. Reset is independent of the polarity of the pulse. That is, regardless of whether a positive narrow pulse is applied or a negative narrow pulse is applied, the resistance of the memory resistor increases with the number of applied pulses, until the resistor reaches its

high resistance state. The same is true for the wide pulse width reset process. Either of a positive wide pulse or a negative wide pulse may be used to re-set the memory resistor to its low resistance state. This feature ~~enable~~ enables the memory to be reset and programmed using single polarity pulses. No bi-polarity power supply is required.

Thus, a non-volatile resistor memory cell fabricated with amorphous PCMO has been disclosed. Amorphous PCMO may be deposited ~~by~~ at low temperature. The thermal budget of amorphous PCMO is compatible with state-of-the-art ULSI integrated circuit processes as the electrode material is also commonly used in the ~~stat-of-the-art~~ state-of-the-art process. The memory device of the invention uses electrical ~~pulse~~ pulses of the same polarity for memory programming and resetting, changing only the pulse duration and number of pulses. Therefore, the amorphous PCMO memory of the invention is suitable for use in embedded memory devices as well as in ultra large-scale memory chip fabrication. The method of the invention and the device of the invention is also applicable to colossal magnetoresistor (CMR), and high temperature super conductor (HTSC) material.

Thus, a method for reversible resistance change induced by electric pulses and a memory device incorporating the method of the invention has been disclosed. It will be appreciated that further variations and modifications thereof may be made within the scope of the invention as defined in the appended claims.